



An Efficient Model for Frequency-Dependent On-Chip Inductance

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Inductance for GHz Designs

- **Interconnect impedance is more than resistance**
 - $Z = R + j\omega L$
 - ω is decided not by the clock frequency, but by clock edge
 - $\omega \approx 1/t_r$
- **On-chip inductance must be considered when ωL is comparable to R**
- **Inductive coupling is a long range effect**

Resistance and Inductance



$L = 2000\mu, W = 0.8\mu, T = 2.0\mu, S = 0.8\mu$

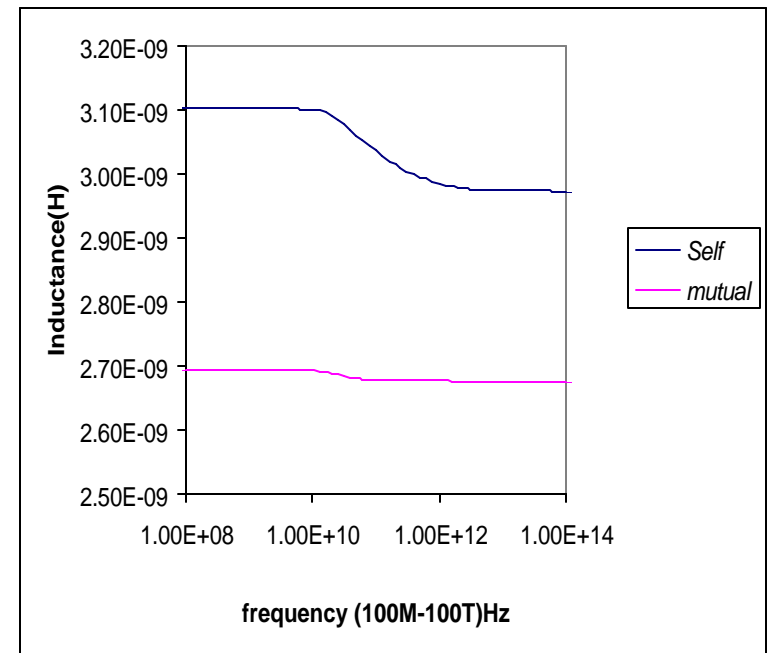
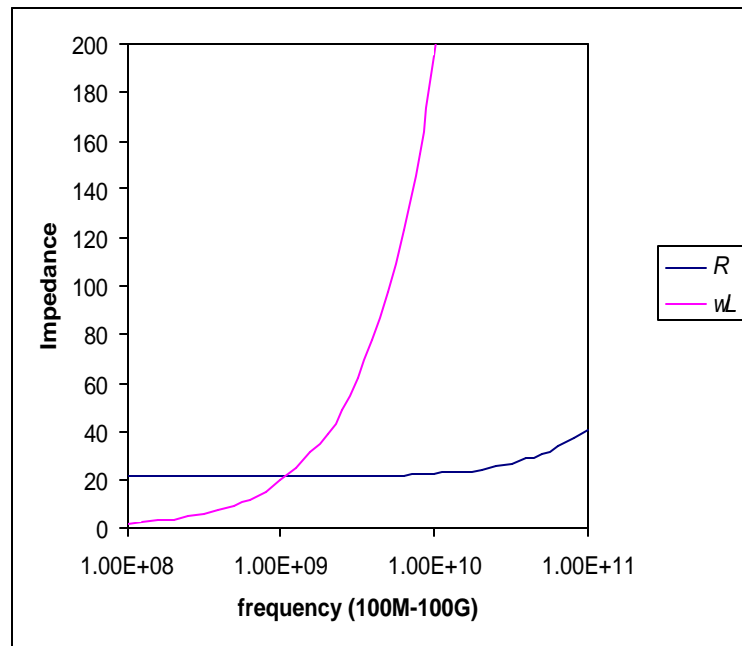


Figure 1: R and wL for a single long wire

Figure 2: L_s and L_x for two parallel wires

Related Work

- **Accurate but slow approach**
 - Numerical extraction (FastHenry: Kamon et. al.94' MTT)
 - Too slow to be applied on whole chip level simulation and design iteration
- **Fast but less accurate approach**
 - Table method for bus structure (He et. al. 99' CICC)
 - Analytical methods for parallel wires (Gala et. al. 00' and Qi et. al. 00')
 - Accurate enough for layout design and verification

Our Contributions

- **Developed a table & formula driven extraction tool**
 - For arbitrary wires
 - Accuracy: $\pm 5\%$ for most cases
 - <http://eda.ece.wisc.edu/WebHenry/>
- **Proposed the so called normalized circuit model to replace full RLC circuit**
 - Experimentally verified their equivalence
 - Less complexity and shorter runtime: 11x speedup in simulation

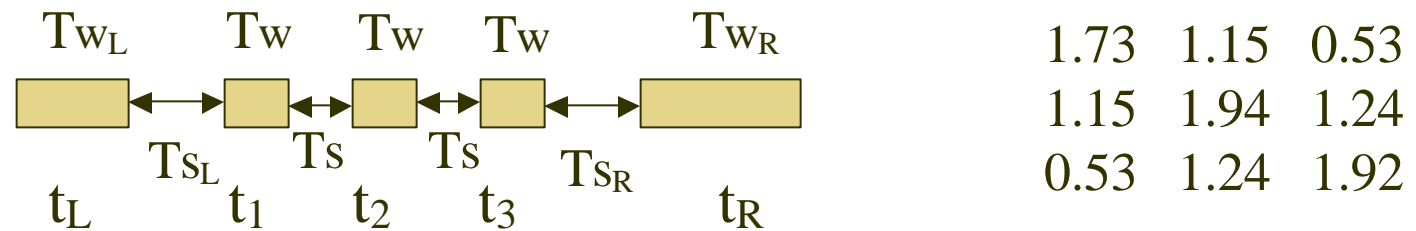
Definition of Loop Inductance



- The loop inductance is

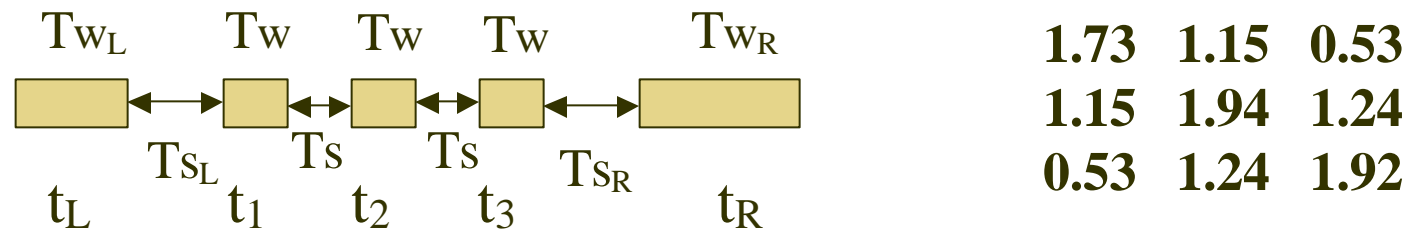
$$L_{ij} = \frac{\mu}{4\pi} \cdot \frac{1}{a_i a_j} \cdot \frac{1}{I_i I_j} \oint_{loop_i} \oint_{loop_j} \frac{1}{r_{ij}} dI_i dI_j da_i da_j$$

Loop Inductance for N Traces



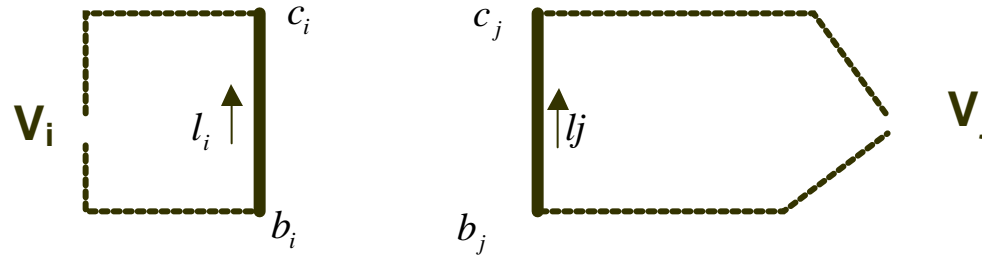
- **Assume edge traces are grounded**
 - leads to 3x3 loop inductance matrix
- **Inductance has a long range effect**
 - e.g., non-negligible coupling between t_1 and t_3 with t_2 between them

Table in Brute-Force Way is Expensive



- **Self inductance has nine dimensions:**
 - (n, length, location, T_{wL} , T_{sL} , T_w , T_s , T_{wR} , T_{sR})
- **Mutual inductance has ten dimensions:**
 - (n, length, location1, location2, T_{wL} , T_{sL} , T_w , T_s , T_{wR} , T_{sR})
- **Length is needed because inductance is not linearly scalable**

Definition of Partial Inductance



- **Partial inductance is the portion of loop inductance for a segment when its current returns via the infinity**
 - called partial element equivalent circuit (PEEC) model
- **If current is uniform, the partial inductance is**

$$L_{ij} = \frac{\mu}{4\pi} \cdot \frac{1}{a_i a_j} \cdot \int_{b_i}^{c_i} \int_{a_i}^{c_j} \int_{b_j}^{a_j} \int \frac{dl_i dl_j}{r_{ij}} da_i da_j$$

Partial Inductance for N Traces

T_{WL}	T_W	T_W	T_W	T_{WR}	6.17	5.43	5.12	4.89	4.66
	T_{SL}	T_S	T_S	T_{SR}	5.43	6.79	6.10	5.48	5.04
t_L	t_1	t_2	t_3	t_R	5.12	6.10	6.79	6.10	5.33
					4.89	5.48	6.10	6.79	5.77
					4.66	5.04	5.33	5.77	6.50

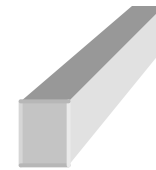
- **Treat edge traces same as inner traces**
 - lead to 5x5 partial inductance table
- **Partial inductance model is more accurate compared to loop inductance model**

Two Foundations

- **By PEEC Definition, He et. al. (CICC '99) pointed out two foundations:**
 - **Self inductance of a wire is solely depended on the wire itself**
 - **Mutual inductance of two wires is solely depended on these two wires themselves**

Table-based approach (He et. al. 99' CICC)

- Inductance table for **parallel** wires
- Self inductance table
 - Length -- L
 - Width -- W
 - Thickness -- T
 - Frequency -- F
- Mutual inductance table
 - L, W, T, F
 - Space -- S

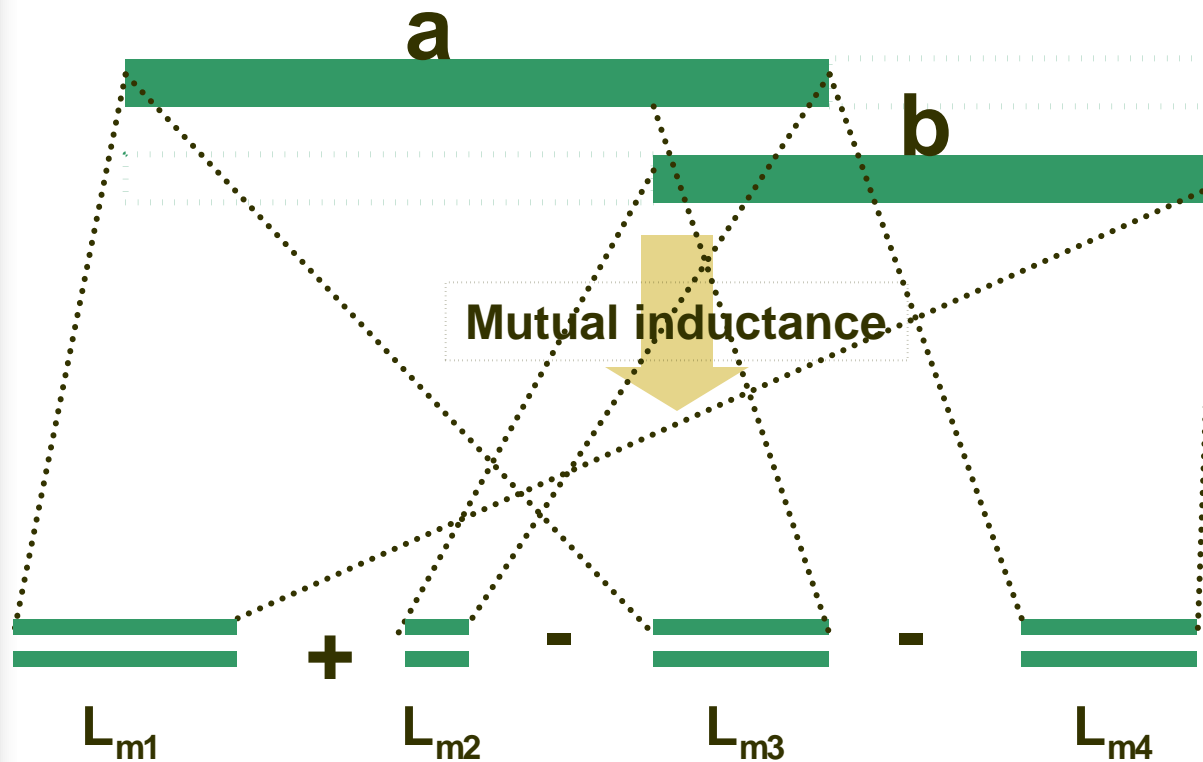


Displaced parallel wires?

- **Based on foundation for mutual inductance:**
 - Solve **ten** dimensional problem
 - $L1, L2, W1, W2, T1, T2, S_v, S_h, D, F$
 - Too big, too slow
- **A formula is proposed to use only **five** dimensional tables**

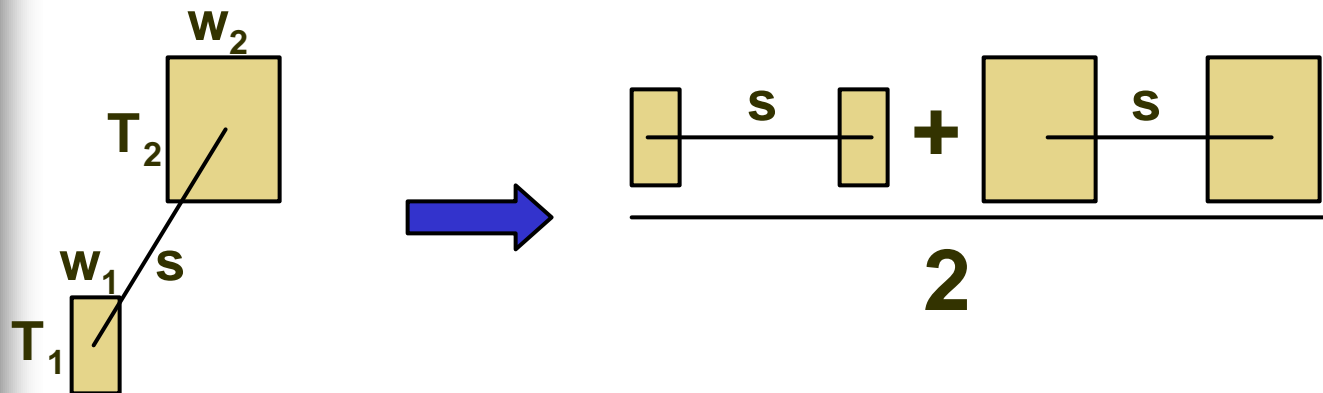
Formula for Lateral Dimension

● $L_{ab} =$

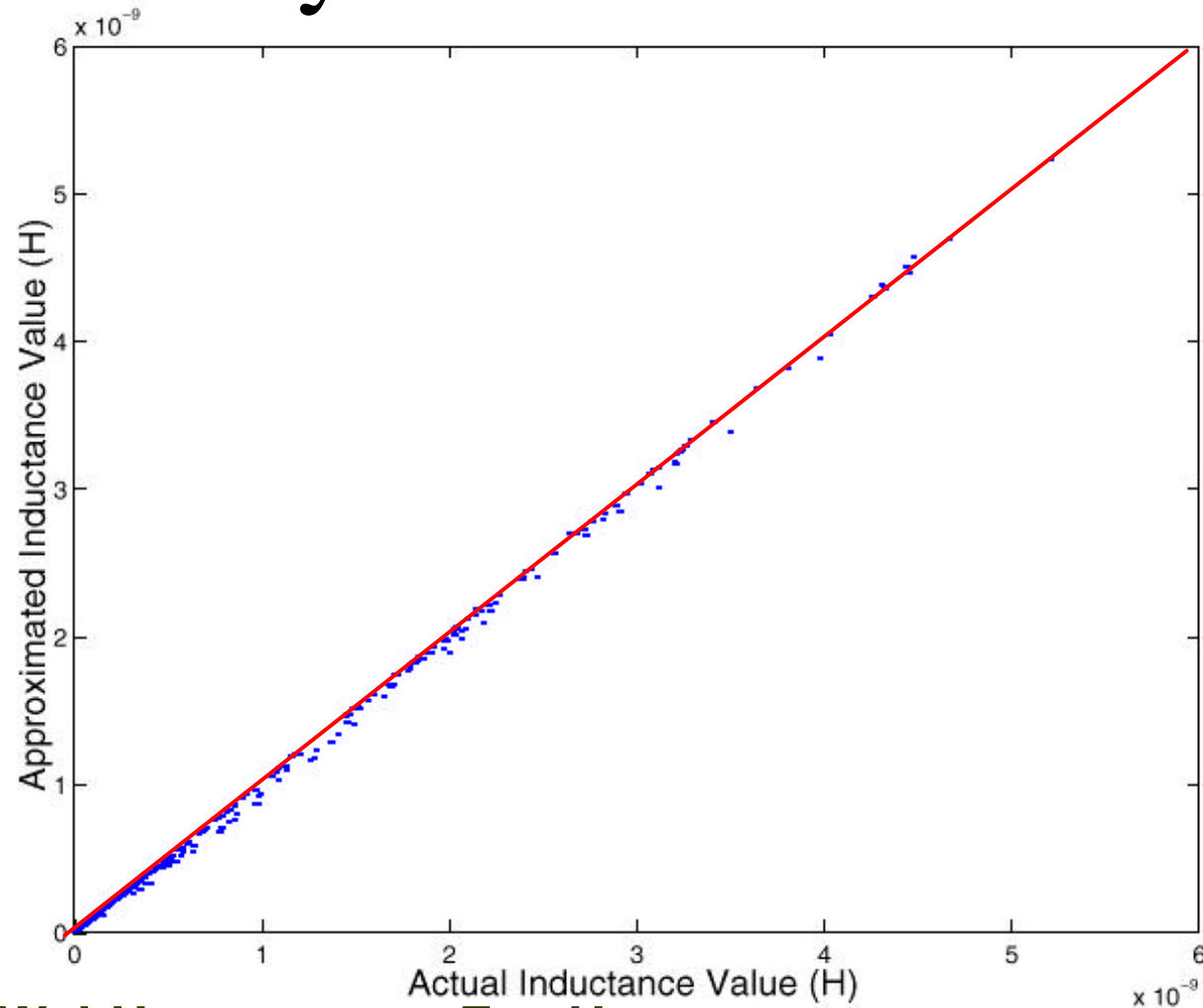


Formula for Cross-section

- **Linear approximation**



Accuracy

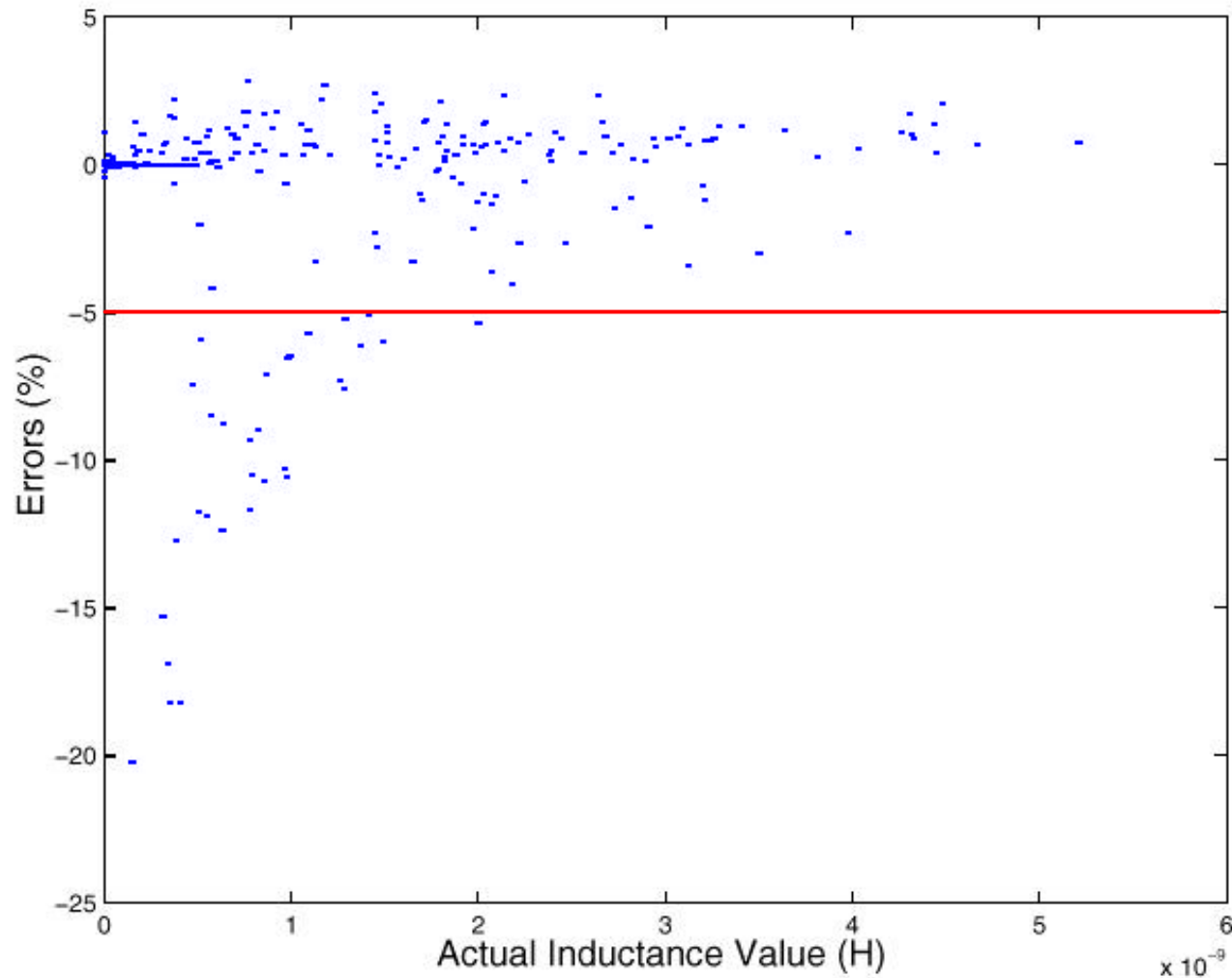


- **WebHenry versus FastHenry**
- **400 random displaced parallel wires cases**

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Error Distribution



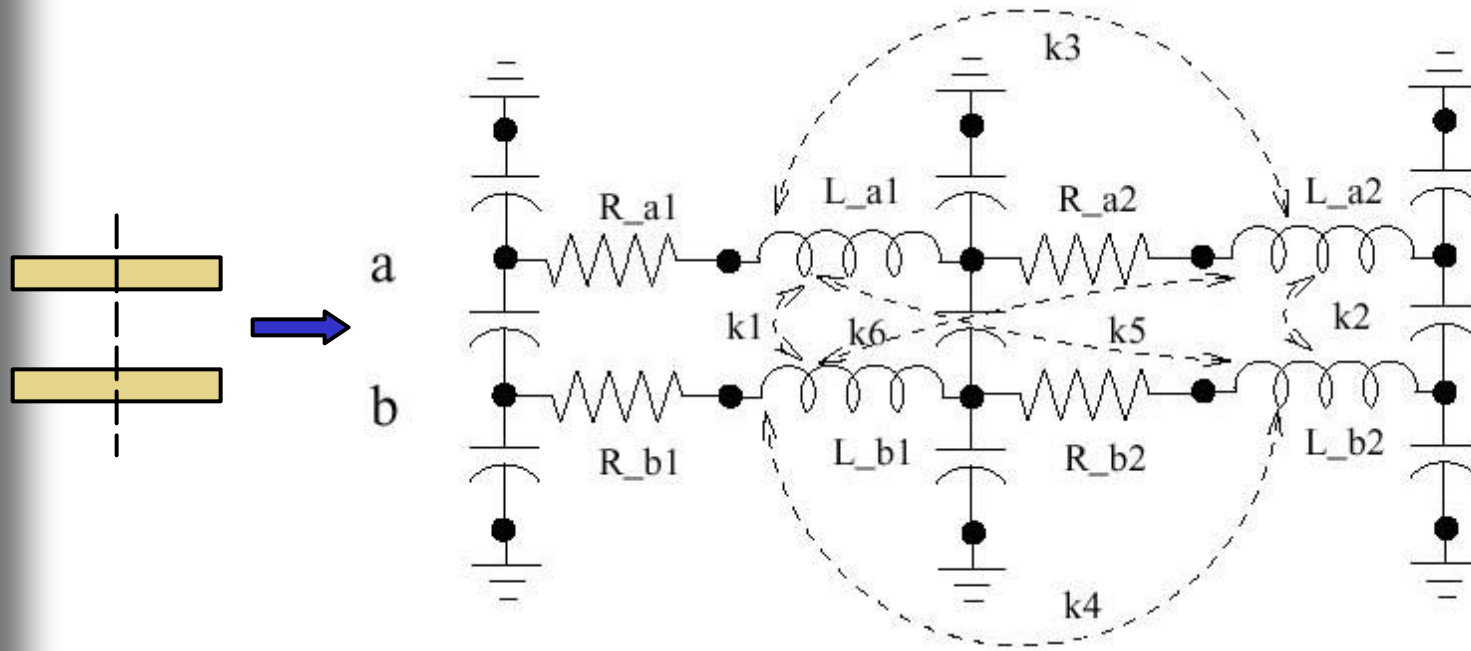
- $\pm 5\%$ most cases
- Bigger error only found in smaller inductance values



Inductance Circuit Modeling

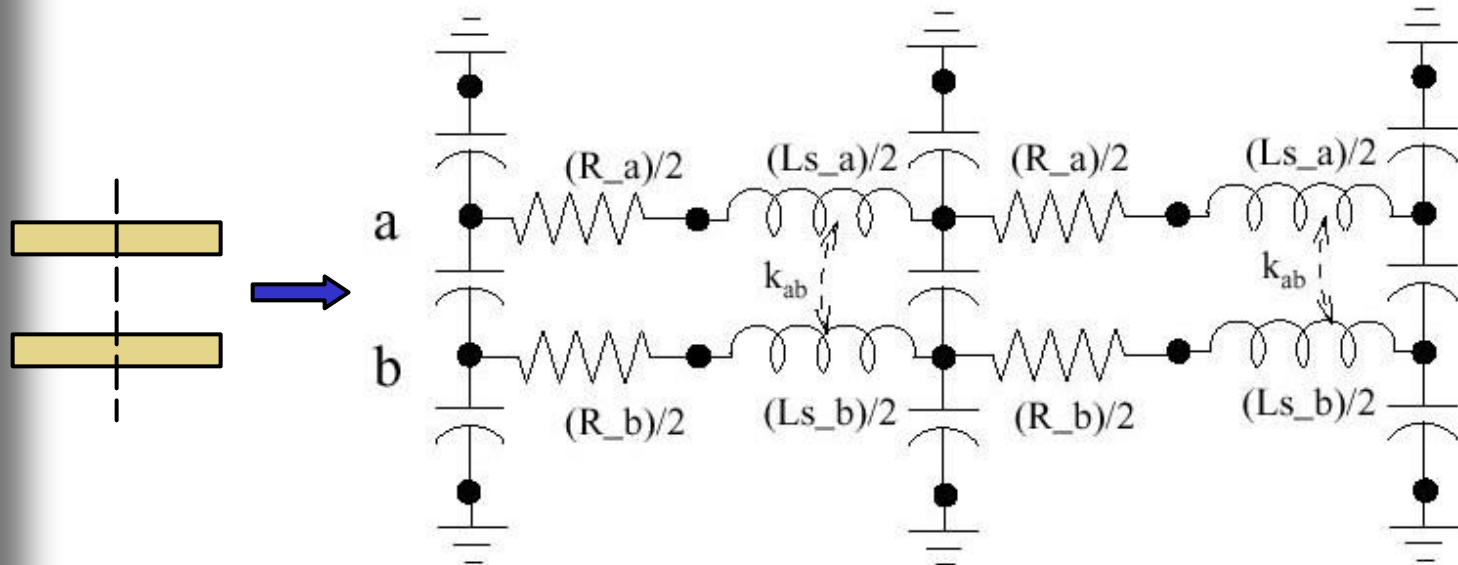
- **Full and normalized circuit model for non-displaced parallel wires**

Full RLC Circuit Model



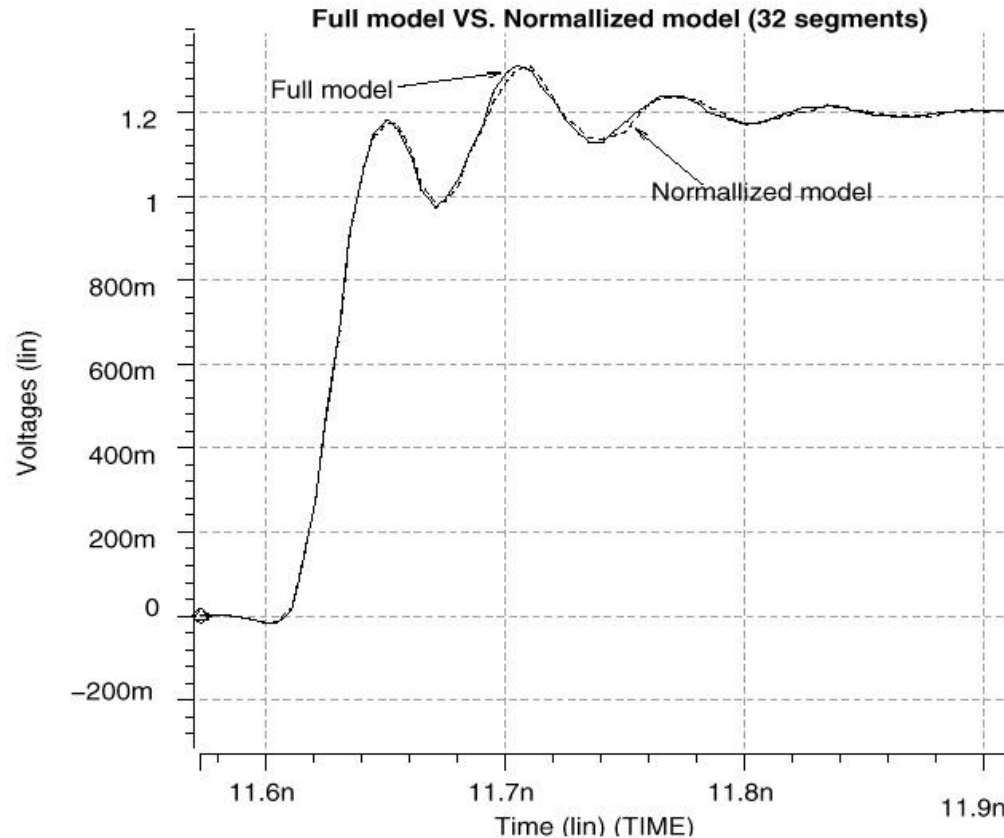
- Linear RC number
- Quadratic L number, $O(n^2)$

Normalized RLC Circuit Model



- Again, linear RC number
- **Linear** L number too!

Full Versus Normalized



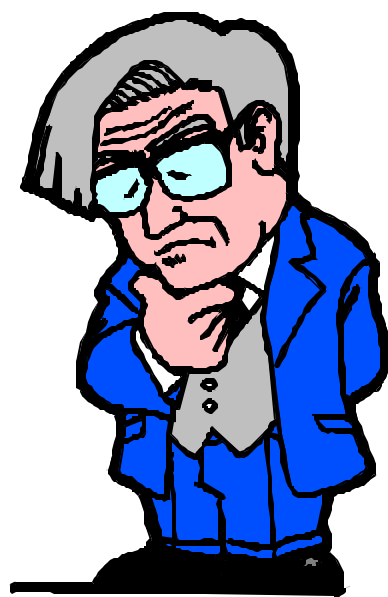
- **Two waveforms are almost identical**
- **Running time:**
 - **Full** **99.0 seconds**
 - **Normalized** **9.1 seconds**

Applications

- **Simultaneous shield insertion and net ordering for signal integrity**
 - [He-Lepak, ISPD'00] [Lepak-et al, DAC'01]
- **Interconnect analysis using decoupling model**
 - [Yin-He, ASP-DAC'01]
- **Simultaneous signal and power routing**
 - [Ma-He, SLIP'01]
-

Conclusion

- **A table-formula driven extraction method is proposed**
 - **Very efficient**
 - **Reasonably accurate**
 - **Frequency dependent**
- **Two circuit models are studied**
 - **Verified the normalized model is accurate and efficient**



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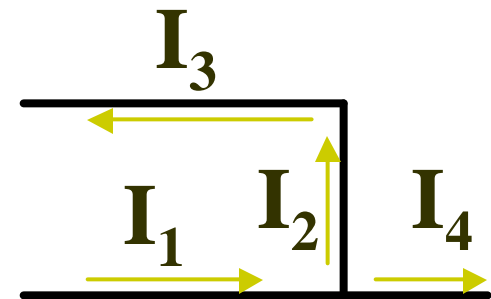
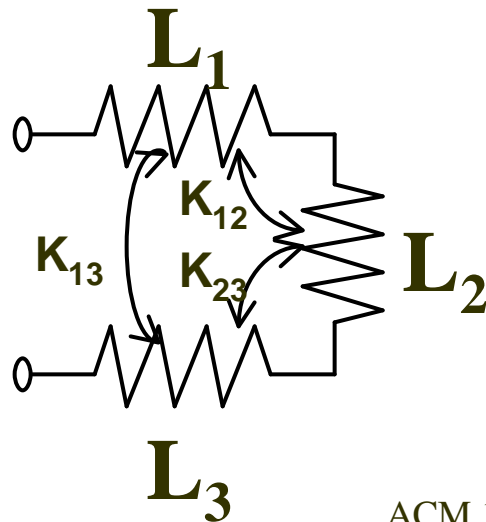
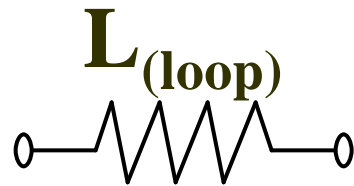
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On-chip Inductance

- **Wire impedance: $Z = R + j\omega L$**
 - Copper interconnects makes $R \ll \omega L$
 - ω is proportional to signal rising time
 - 1 GHz clock $\omega = 2\pi \cdot 10\text{GHz}$
- **Inductive coupling is a long range effect**
- **Partial inductance model is preferred.**
Let the circuit simulator to determine the signal return path

The PEEEC Model

- **Eliminate the current return path problem**



Assume current return from infinite